

AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1 - 16. (Canceled)

17. (Currently Amended) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

~~an insulator layer overlying a semiconductor substrate;~~

~~polysilicon traces overlying said insulator layer;~~

10 a liner oxide layer overlying said polysilicon trace traces wherein said liner oxide layer covers sidewalls of said polysilicon trace ~~traces on edges where~~ at said source and drain regions ~~are planned~~ and wherein said liner oxide layer covers the top of said polysilicon trace; and

15 silicon nitride spacers wherein said liner oxide layer is

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laterally between said silicon nitride spacers and said
polysilicon trace at said source and drain regions on
~~sidewalls of said polysilicon traces and overlying said~~
~~liner oxide layer and~~ wherein said silicon nitride spacer
20 have an L-shaped profile, ~~and~~
~~an interlevel dielectric layer overlying said~~
~~polysilicon traces, said silicon nitride spacers, and said~~
~~liner oxide layer.~~

18. (Original) The device according to Claim 17 wherein
said liner oxide layer has a thickness of between about 50
Angstroms and 300 Angstroms.

19. (Canceled)

20. (Original) The device according to Claim 17 wherein
said interlevel dielectric layer comprises a combination
material from the group of: TEOS undoped oxide, boron
phosphosilicate glass (BPSG), undoped silicon dioxide,
5 silicon nitride, and silicon oxynitride.

21. (Previously Presented) The device according to Claim

17 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

22. (Currently Amended) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

~~an insulator layer overlying a semiconductor substrate;~~

~~polysilicon traces overlying said insulator layer wherein said polysilicon traces comprise transistor gates;~~

a liner oxide layer overlying said polysilicon trace
~~traces~~ wherein said liner oxide layer covers sidewalls of said polysilicon trace ~~traces on edges where~~ at said source and drain regions are planned and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions, on
~~sidewalls of said polysilicon traces and overlying said~~

20 ~~liner oxide layer~~ wherein said silicon nitride spacers have
an L-shaped profile, and wherein said silicon nitride layer
is formed by one of the group of: growing by thermal
process. ~~and~~

~~an interlevel dielectric layer overlying said~~
25 ~~polysilicon traces, said silicon nitride spacers, and said~~
~~liner oxide layer.~~

23. (Previously Presented) The device according to Claim
22 wherein said liner oxide layer has a thickness of
between about 50 Angstroms and 300 Angstroms.

24. (Previously Presented) The device according to Claim 22
wherein said interlevel dielectric layer comprises a
combination material from the group of: TEOS undoped oxide,
boron phosphosilicate glass (BPSG), undoped silicon
5 dioxide, silicon nitride, and silicon oxynitride.

25. (Canceled)

26. (Currently Amended) A MOSFET device comprising:
a gate comprising a polysilicon trace overlying a
semiconductor substrate with an insulator therebetween;
a source region and a drain region in said

5 semiconductor substrate with said polysilicon trace
laterally between said source and drain regions;
 ~~an insulator layer overlying a semiconductor~~
~~substrate;~~
 ~~polysilicon traces overlying said insulator layer~~
10 ~~wherein said polysilicon traces comprise transistor gates;~~
 a liner oxide layer overlying said polysilicon trace
~~traces~~ wherein said liner oxide layer covers sidewalls of
said polysilicon trace ~~traces on edges where~~ at said source
and drain regions ~~are planned~~ and wherein said liner oxide
15 layer covers the top of said polysilicon trace; and
 silicon nitride spacers wherein said liner oxide layer
is laterally between said silicon nitride spacers and said
polysilicon trace at said source and drain regions, ~~on~~
~~sidewalls of said polysilicon traces and overlying said~~
20 ~~liner oxide layer~~ wherein said silicon nitride spacers have
an L-shaped profile, and wherein said silicon nitride layer
is formed by chemical vapor deposition, ~~and~~
 ~~an interlevel dielectric layer overlying said~~
~~polysilicon traces, said silicon nitride spacers, and said~~
25 ~~liner oxide layer.~~

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27. (Previously Presented) The device according to Claim 26 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

28. (Previously Presented) The device according to Claim 26 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon
5 dioxide, silicon nitride, and silicon oxynitride.